

TEST REPORT

IEC 62116

Test procedure of islanding prevention measures for utilityinterconnected photovoltaic inverters

Report Number. GZES200601936102

Date of issue: 23/06/2020

Total number of pages 14

Name of Testing Laboratory

Branch

Applicant's name...... Shenzhen SOFAR SOLAR Co., Ltd.

Community, XinAn Street, BaoAn District, Shenzhen City,

Guangdong Province, P.R. China

Test specification:

Standard :: IEC/EN 62116: 2014 (Second Edition)

Test procedure....: Characteristic Examination

Non-standard test method.....: N/A

Test Report Form No.....: IEC62116B

Test Report Form(s) Originator....: TÜV SÜD Product Service GmbH

Master TRF....:: Dated 2014-10

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Hybrid Inverter (Three Phase) Test item description.....: Trade Mark: **5** FAR

Manufacturer....: Shenzhen SOFAR SOLAR Co., Ltd.

401, Building 4, AnTongDa Industrial Park, District 68, XingDong Address::

Community, XinAn Street, BaoAn District, Shenzhen City, Guangdong Province, P.R. China

HYD 5KTL-3PH, HYD 6KTL-3PH, HYD 8KTL-3PH; Model/Type reference.....:

HYD 10KTL-3PH, HYD 15KTL-3PH, HYD 20KTL-3PH;

Ratings:: See model list in Page 7 to Page 8.

Serial Number: SP1ES020H71002

Firmware version: V2.00



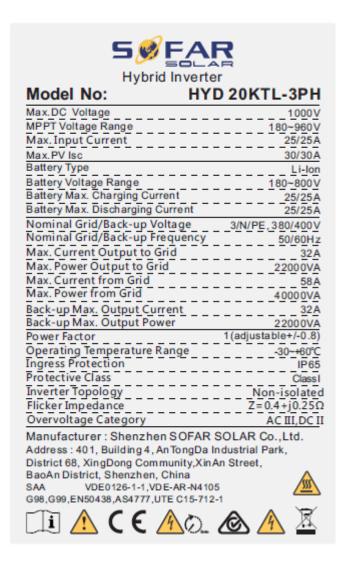
Respo	nsible Testing Laboratory (as applicable), testing procedure a	nd testing location(s):	
	CB Testing Laboratory:			
Testing	g location/ address :			
	Associated CB Testing Laboratory:			
Ø	Testing procedure: TMP/CTF Stage 1:	Shenzhen SOFAR SO	LAR Co., Ltd.	
Testing	g location/ addressskings CO.LID	401, Building 4, AnTongDa Industrial Park, District 68, XingDong Community, XinAn Street, BaoAn District, Spenzhen City, Guangdong Province, P.R. China		
Tested	I by (name, function, signature):	Hugo zhang (Project Engineer)	11 ufo 2 houng	
Approv	ved by (name, function, signature: 💉	Roger Hu	Romber	
	*	(Project Engineer)	Regula	
	Testing procedure: WMT/CTF Stage 2:			
	Testing procedure: SMT/CTF Stage 3 or 4:			



	50	Hz	
Attachment #	Descrip	otion	Pages
Attachment I	Pictures of the EUT and Ele	ctrical Schemes	10 pages
Attachment II	Graphics of the Test Results	S	3 pages
Attachment III	Graphics of the Islanding Be	ehavior Detection	19 pages
Attachment IV	Testing Information		9 pages
Summary of testing:			
Tests performed (nar	ne of test and test clause):	Testing location:	
		Shenzhen SOFAR S	SOLAR Co., Ltd.
All clauses except:		401, Building 4, AnT	ongDa Industrial Park, District 68
- Sub-clause d) of the Voltage and frequent	Table 5 of the point 6.1. ency trips shall be adjusted onal Standards and/or loca	XingDong Communi Shenzhen City, Gua	tv. XinAn Street. BaoAn District.
	pection and tests performed or we conclude that it complies of the Standard		



Copy of marking plate(representative):



Note:

- The above markings are the minimum requirements required by the safety standard. For the final
 production samples, the additional markings which do not give rise to misunderstanding may be added.
- 2. Label is attached on the side surface of enclosure and visible after installation
- 3. Labels of other models are as the same with HYD 20KTL-3PH's except the parameters of rating.



Test item particulars:	Solar Grid-tied Inverter (Three Phase Inverter)				
Classification of installation and use:	Fixed (permanent connection)				
Supply Connection:	DC; PV				
:	AC; Grid connection				
Possible test case verdicts:					
- test case does not apply to the test object:	N/A				
- test object does meet the requirement:	P (Pass)				
- test object does not meet the requirement:	F (Fail)				
Testing:	CTF Stage 1 procedure				
Date of receipt of test item:	N/A				
Date (s) of performance of tests:	From 29/05/2020 and 01/06/2020				
General remarks:					
"(See Enclosure #)" refers to additional information appended to the report. "(See appended table)" refers to a table appended to the report. This document is issued by the Company subject to its General Conditions of Service printed overleaf, available on request or accessible at www.sgs.com/terms_and_conditions.htm and, for electronic format documents, subject to Terms and Conditions for Electronic Documents at www.sgs.com/terms_e-document.htm . Attention is drawn to the limitation of liability, indemnification and jurisdiction issues defined therein. Any holder of this document is advised that information contained hereon reflects the Company's findings at the time of its intervention only and within the limits of Client's instructions, if any. The Company's sole responsibility is to its Client and this document does not exonerate parties to a transaction from exercising all their rights and obligations under the transaction documents. This document cannot be reproduced except in full, without prior written approval of the Company. Any unauthorized alteration, forgery or falsification of the content or appearance of this document is unlawful and offenders may be prosecuted to the fullest extent of the law. Unless otherwise stated the results shown in this test report refer only to the sample(s) tested. Throughout this report a comma / point is used as the decimal separator.					
Manufacturer's Declaration per sub-clause 4.2.5 of I	ECEE 02:				
The application for obtaining a CB Test Certificate includes more than one factory location and a declaration from the Manufacturer stating that the sample(s) submitted for evaluation is (are) representative of the products from each factory has been provided	☐ Yes ☑ Not applicable				
When differences exist; they shall be identified in the	e General product information section.				
Name and address of factory (ies):	Dongguan SOFAR SOLAR Co.,Ltd. 1F - 6F, Building E, No. 1 JinQi Road, Bihu Industrial Park, Wulian Village, Fenggang Town, Dongguan City, Guangdong Province,P.R. China.				



General product information:

Product covered by this report is grid-connected PV inverter for indoor or outdoor installation. The connection to the DC input and AC output are through connectors.

The Solar inverter converts DC voltage into AC voltage.

The input and output are protected by varistors to Earth. The unit is providing EMC filtering at the output toward mains. The unit does not provide galvanic separation from input to output (transformerless). The output is switched off redundant by the high power switching bridge and a two relays. This assures that the opening of the output circuit can operate in case of one error.

Equipment Under Testing:

- HYD 20KTL-3PH;

Variant models:

- HYD 5KTL-3PH;
- HYD 6KTL-3PH;
- HYD 8KTL-3PH;
- HYD 10KTL-3PH;
- HYD 15KTL-3PH;

ModelHYDHYDHYD5KTL-3PH6KTL-3PH8KTL-3PH1		HYD 10KTL-3PH	HYD 15KTL-3PH	HYD 20KTL-3PH					
		P	V String Input Da	ata					
Recommended- Max.PV power									
Max. DC voltage		1000V							
Start-up operating voltage			2	200V					
MPPT voltage range			180	V~960V					
Nominal DC voltage			6	500V					
Full power MPPT voltage range	250V~850V	320V~850V	360V~850V	220V~850V	350V~850V	450V~850V			
Max. input current	12.5A/12.5A	12.5A/12.5A	12.5A/12.5A	25A/25A	25A/25A	25A/25A			
Max. short current	15A/15A	15A/15A	15A/15A	30A/30A	30A/30A	30A/30A			
		E	Battery Input Da	ta					
Battery voltage range			180	V~800V					
Battery voltage range for full load	200V~800V	240V~800V	320V~800V	200V~800V	300V~800V	400V~800V			
No. of battery 1			2						
Nominal charging/dischar- ging power	5000W	6000W	8000W	10000W	15000W	20000W			
Max. charging/dischar- ging current	25A	25A	25A	50A (25A/25A)	50A (25A/25A)	50A (25A/25A)			



Page 8 of 14

Peak charging/dischar- ging current, Duration	40A, 60s	40A, 60s	40A, 60s	70A (35A/35A), 60s	70A (35A/35A), 60s	70A (35A/35A), 60s		
		AC (Dutput Data (On	ı-grid)				
Nominal AC power	5000W	6000W	8000W	10000W	15000W	20000W		
Max. AC power output to utility grid	5500VA	6600VA	8800VA	11000VA	16500VA	22000VA		
Max. AC power from utility grid	10000VA	12000VA	16000VA	20000VA	30000VA	40000VA		
Max. AC current output to utility grid	8A	10A	13A	16A	24A	32A		
Max. AC Current from utility grid	15A	17A	24A	29A	44A	58A		
		AC C	Dutput Data (Ba	ck-up)				
Nominal output power	5000W	6000W	8000W	10000W	15000W	20000W		
Max. output power	5500VA	6600VA	8800VA	11000VA	16500VA	22000VA		
Peak output power, Duration	10000VA, 60s	12000VA, 60s	16000VA, 60s	20000VA, 60s	22000VA, 60s	22000VA, 60s		
Max. output current	8A	10A	13A	16A	24A	32A		
Peak output current, Duration	15A, 60s	18A, 60s	24A, 60s	30A, 60s	32A, 60s	32A, 60s		
Nominal output voltage			3/N/PE, 220/38	30Vac, 230/400V	′ac			
Nominal output freqency			50)/60Hz				
Output power factor			~1(0.8 leadir	ng to 0.8 lagging))			
Operating temperature range		-30°C ~60°C						
Ingress protection				IP65				
Protective class		1	C	lass I				
Cooling method	heat sink	heat sink	heat sink	fan	fan	fan		

The variants models have been included in this test report without tests because the following features don't change regarding to the tested model:

- Same connection system and hardware topology
- Same control algorithm.
- Same Firmware Version



	IEC 62116		
Clause	Requirement + Test	Result - Remark	Verdict
4	Testing circuit		
	The testing circuit shown in Figure 1 is employed.		Р
	Similar circuits are used for three-phase output.		Р
	Parameters to be measured are shown in Table 1		Р
	and Figure 1. Parameters to be recorded in the test		
	report are discussed in Clause 7.		
5	Testing equipment		
5.1	Measuring instruments		Р
	The waveform measurement/capture device is able	Oscillograph and Power	Р
	to record the waveform from the beginning of the	analyzer equipped with	
	islanding test until the EUT ceases to energize the	memory function	
	island.	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	
		Waveform caught from the	
		switch open and the EUT cease to energize	
	For multi-phase EUT, all phases are monitored.	Cease to energize	P
	A waveform monitor designed to detect and	See Annex IV for testing	P P
	calculate the run-on time may be used.	equipment information	'
	For multi-phase EUT, the test and measurement	equipment imorniation	Р
	equipment is recorded each phase current and each		· ·
	phase-to-neutral or phase-to-phase voltage, as		
	appropriate, to determine fundamental frequency		
	active and reactive power flow over the duration of		
	the test.		
	A sampling rate of 10 kHz or higher is	Less than 1% of the rated	Р
	recommended. The minimum measurement	EUT output current	
	accuracy is 1 % or less of rated EUT nominal output		
	voltage and 1 % or less of rated EUT output current		
	Current, active power, and reactive power		P
	measurements through switch S1 used to determine		
	the circuit balance conditions report the fundamental		
5.2	(50 Hz or 60 Hz) component.		
5.2.1	DC power source General	<u> </u>	П
3.2.1	A PV array or PV array simulator (preferred) may be	Chroma PV simulator used	P
	used. If the EUT can operate in utility-	Ciliona F v simulator used	
	interconnected mode from a storage battery, a DC		
	power source may be used in lieu of a battery as		
	long as the DC power source is not the limiting		
	device as far as the maximum EUT input current is		
	concerned.		<u> </u>
	The DC power source provides voltage and current		Р
	necessary to meet the testing requirements		1
	described in Clause 6.		
5.2.2	PV array simulator		P
	The tests are conducted at the input voltage defined		Р
	in Table 2 below, and the current is limited to 1,5		
	times the rated photovoltaic input current, except		1
	when specified otherwise by the test requirements.	 	+
	A PV array simulator is recommended, however,		P
	any type of power source may be used if it does not influence the test results.		
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	IEC 62116						
Clause	Requirement + Test		Result - Remark	Verdict			
	'						
5.2.3	Current and voltage limi with series resistance	ted DC power supply		N/A			
		as the EUT input source is		N/A			
	capable of EUT maximum						
	achieve EUT maximum ou						
	and maximum EUT input			N1/A			
	The power source provide voltage limit, set to provide			N/A			
	current and open circuit vo						
	with the series and shunt						
	below.						
	A series resistance (and, o			N/A			
	resistance) is selected to	provide a fill factor within					
	the range:						
	Output power: Sufficient to						
	output power and other level conditions of table 5.	veis specified by test					
	Response speed: The res	ponse time of a simulator					
	to a step in output voltage						
	change, results in a settlin						
	within 10% of its final valu						
	Stability: Excluding the val						
	EUT MPPT, simulator out	wer level over the duration					
	of the test: from the point						
	achieved until the island o						
	allowable run-on time is ex						
	Power factor: 0.25 to 0.8						
5.2.4	PV array			N/A			
		JT input source is capable		N/A			
	of EUT maximum input po						
	maximum EUT input opera	ating voltage. when the irradiance varies		N/A			
		the duration of the test as		IN/A			
	measured by a silicon-type						
	reference device. It may be						
	array configuration to achi	, ,					
	power levels prescribed in	6.1.					
5.3	AC power source						
	The utility grid or other AC		AC power source used meets	Р			
	•		the conditions specified				
	Table 4.	source requirements					
	Items	Conditions					
	Voltage	Nominal ±2,0 %					
	Voltage THD	< 2,5 %					
	Phono code dictores 1)	Nominal ±0,1 Hz					
	Phase angle distance 1) 1) Three-phase case only	120 ° ± 1,5 °					
5.4	AC loads						
J. 4	I AC IDAUS						



	IEC 62116	Report No. GZE5200	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
		1	
Clause	Requirement + Test	Result - Remark	Verdict
	On the AC side of the EUT, variable resistance,	Passive loads (variable	Р
	capacitance, and inductance are connected in	resistance, capacitance and	
	parallel as loads between the EUT and the AC	inductance) have been	
	power source. Other sources of load, such as	connected.	
	electronic loads, may be used if it can be shown that		
	the source does not cause results that are different		
	than would be obtained with passive resistors,		
	inductors, and capacitors.		
	All AC loads are rated for and adjustable to all test		Р
	conditions. The equations for Qf are based upon an		
	ideal parallel RLC circuit. For this reason, non-		
	inductive resistors, low loss (high Qf) inductors,		
	and capacitors with low effective series resistance		
	and effective series inductance are utilized in the		
	test circuit. Iron core inductors, if used, are not		
	exceed a current THD of 2 % when operated at		
	nominal voltage. Load components are		
	conservatively rated for the voltage and power		
	levels expected. Resistor power ratings are chosen		
	so as to minimize thermally-induced drift in		
	esistance values during the course of the test.		P
	Active and reactive power is calculated (using the		P
	measurements provided in Table 1) in each of the		
	R, L and C legs of the load so that these parasitic parameters (and parasitics introduced by variacs or		
	autotransformers) are properly accounted for when		
	calculating Qf.		
6	Test for single or multi-phase inverter		
6.1	Test procedure	(see appended table)	Р
-	The test uses an RLC load, resonant at the EUT	(сее принаса насе,	_
			Р
			Р
	nominal frequency (50 Hz or 60 Hz) and matched to		Р
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power.		·
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all		P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all		·
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases		·
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in		P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given		P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating.		P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power		P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source		P P P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source c) Turn off the EUT and open S1		P P P P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source c) Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05		P P P P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source c) Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e) Connect the RLC load configured in step d) to		P P P P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source c) Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e) Connect the RLC load configured in step d) to the EUT by closing S2		P P P P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source c) Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e) Connect the RLC load configured in step d) to the EUT by closing S2 f) Open the utility-disconnect switch S1 to initiate		P P P P P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source c) Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e) Connect the RLC load configured in step d) to the EUT by closing S2 f) Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded.		P P P P P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source c) Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e) Connect the RLC load configured in step d) to the EUT by closing S2 f) Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. g) For test condition A, adjust the real load and only		P P P P P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source c) Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e) Connect the RLC load configured in step d) to the EUT by closing S2 f) Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. g) For test condition A, adjust the real load and only one of the reactive load components to each of		P P P P P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source c) Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e) Connect the RLC load configured in step d) to the EUT by closing S2 f) Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. g) For test condition A, adjust the real load and only one of the reactive load components to each of the load imbalance conditions shown in the		P P P P P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source c) Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e) Connect the RLC load configured in step d) to the EUT by closing S2 f) Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. g) For test condition A, adjust the real load and only one of the reactive load components to each of the load imbalance conditions shown in the shaded portion of table 6. If any of the recorded		P P P P P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source c) Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e) Connect the RLC load configured in step d) to the EUT by closing S2 f) Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. g) For test condition A, adjust the real load and only one of the reactive load components to each of the load imbalance conditions shown in the shaded portion of table 6. If any of the recorded run-on times are longer than the one recorded		P P P P P
	nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a) Determine EUT test output power b) Adjusting the DC input source c) Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e) Connect the RLC load configured in step d) to the EUT by closing S2 f) Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. g) For test condition A, adjust the real load and only one of the reactive load components to each of the load imbalance conditions shown in the shaded portion of table 6. If any of the recorded		P P P P P



	Page 12 01 14	Report No. GZES200	00 1000 102
	IEC 62116		
Clause	Requirement + Test	Result - Remark	Verdict
	1 '		
	h) For test condition B and C, adjust the only one		Р
	reactive load components by approximately 1,0%		
	per test, within a total range of 95% to 105% of the		
	operating point. If run-on times are still increasing at		
	the 95% or 105% points, additional 1% increments		
	have to be taken until run-on times begin		
	decreasing.		
6.2	Pass/fail criteria	T=	
	An EUT is considered to comply with the	Run-on time is less than 2s in	Р
	requirements for islanding protection when each	any case	
	case of recorded run-on time is less than 2 s or		
-	meets the requirements of local codes.		
7	Documentation At a minimum, the fellowing information is recorded.		Р
	At a minimum, the following information is recorded		P
	and maintained in the test report.		P
	a) Specifications of EUT. Table 8 provides an example of the type of information that is provided.		
	b) Measurement results. Table 9 provides an		Р
	example of the type of information that is provided.		!
	Actual measured values is to be recorded.		
	c) Block diagram of test circuit.		Р
	d) Specifications of the test and measurement		P
	equipment. Table 10 provides an example of the		
	type of information that is provided.		
	e) Any test configuration or procedure details such		Р
	as methods of achieving specified load and EUT		
	output conditions.		
	f) Any additional information required by the testing		Р
	laboratory's accreditation.		
	g) Specify the evaluation criterion from clause 6.2		Р
	that was utilized to determine if the product passed		
Δ	or failed the test.		
Annex A	Islanding as it applies to PV systems(Informative)		
A.1	General		
A.2	Impact of distortion on islanding	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	
Annex B	Test for independent islanding detection device (rela	y)(mormative)	
B.1 B.2	Introduction Testing circuit		
B.3	Testing circuit Testing equipment		
B.4	Testing equipment Testing procedure		
B.5	Documentation		
ט.ט	Documentation		





Report No. GZES200601936102

		9				
IEC 62116						
Clause	Requirement + Test		Result - Remark	Verdict		

6.1 Table: tested condition and run-on time

No.	P _{EUT} (% of	Reactive	P _{AC}	Q_{AC}	Run-on	P _{EUT}	Actual Q _f	V_{DC}	Which load
110.	EUT	load (% of	I AC	Q AC	time(ms)	(KW)	Actual Q	(d.c.V)	is selected to be
	rating)	normial)							adjusted (R
				Test co	ndtion A				or L)
1	100	100	0	0	544	20.1	1.01	808.2	
2	100	100	-5	-5	404	20.2	1.05	808.6	R/L
3	100	100	-5	0	436	20.1	1.05	808.7	R
4	100	100	-5	+5	410	20.2	1.03	808.2	R/L
5	100	100	0	-5	482	20.1	1.02	8.808	L
6	100	100	0	+5	510	20.1	1.05	808.6	L
7	100	100	+5	-5	412	20.1	0.98	809.1	R/L
8	100	100	+5	0	442	20.2	0.96	808.3	R
9	100	100	+5	+5	414	20.1	0.96	808.5	R/L
10	100	100	-10	+10					R/L
11	100	100	-5	+10					R/L
12	100	100	0	+10					L
13	100	100	+10	+10					R/L
14	100	100	+10	+5					R/L
15	100	100	+10	0					R
16	100	100	+10	-5		-		-	R/L
17	100	100	+10	-10					R/L
18	100	100	+5	-10		-		-	R/L
19	100	100	+5	10					R/L
20	100	100	0	-10					L
21	100	100	-5	-10		-		-	R/L
22	100	100	-10	-10				-	R/L
23	100	100	-10	-5					R/L
24	100	100	-10	0				-	R/L
25	100	100	-10	+5				-	R/L



Report No. GZES200601936102



IEC 62116					
Clause	Requirement + Test	Result - Remark	Verdict		

Test condtion B									
10	66	66	0	0	496	13.2	1.00	571.2	
11	66	66	0	-5	418	13.2	1.02	571.8	L
12	66	66	0	-4	430	13.2	1.02	571.7	L
13	66	66	0	-3	444	13.2	1.02	571.4	L
14	66	66	0	-2	446	13.2	1.01	572.0	L
15	66	66	0	-1	462	13.2	1.00	571.6	L
16	66	66	0	1	490	13.2	1.00	571.8	L
17	66	66	0	2	468	13.2	0.99	572.1	L
18	66	66	0	3	458	13.2	0.98	571.8	L
19	66	66	0	4	452	13.2	0.98	571.9	L
20	66	66	0	5	404	13.2	0.97	571.3	L
21	66	66	0	6					L
Test condition C									
22	33	33	0	0	518	6.6	1.00	328.3	
23	33	33	0	-5	380	6.6	1.03	328.4	L
24	33	33	0	-4	442	6.6	1.02	328.9	L
25	33	33	0	-3	448	6.6	1.02	329.0	L
26	33	33	0	-2	466	6.6	1.01	328.5	L
27	33	33	0	-1	482	6.6	1.01	328.3	L
28	33	33	0	1	508	6.6	1.00	328.2	L
29	33	33	0	2	444	6.6	0.99	329.1	L
30	33	33	0	3	424	6.6	0.99	328.8	L
31	33	33	0	4	422	6.6	0.98	328.6	L
32	33	33	0	5	396	6.6	0.97	328.4	L
33	33	33	0	6					L

Remark:

For test condition A:

If any of the recorded run-on times are longer than the one recorded for the rated balance condition, then the non-shaded parameter combinations also require testing.

For test condition B and C:

If run-on times are still increasing at the 95 % or 105 % points, additional 1 % increments is taken until runon times begin decreasing.

--- End of test report---



Page 1 of 10

IEC 62116:2014 (50Hz)

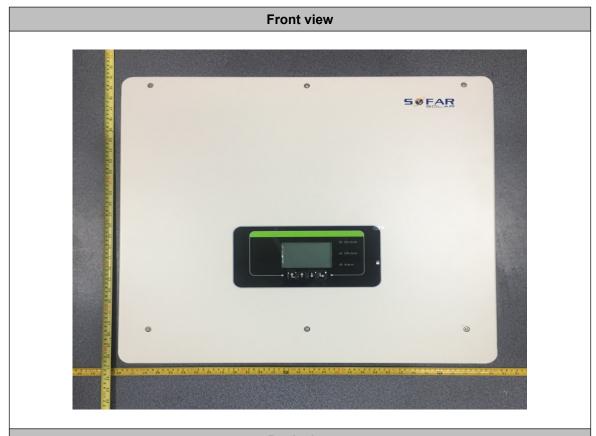
ATTACHMENT I

(Pictures of the EUT and Electrical Schemes)

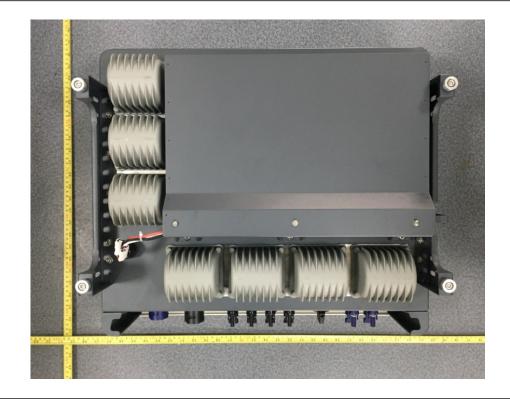


IEC 62116:2014 (50Hz)

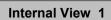
1 PICTURES



Back view









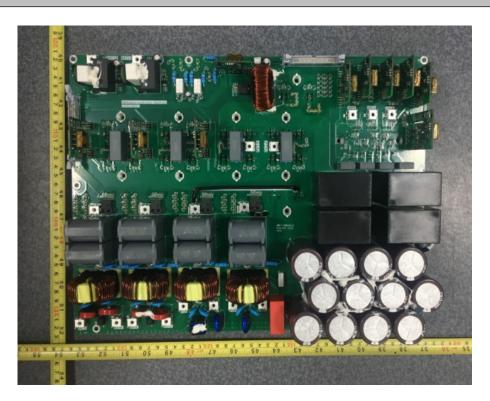
Internal View 2



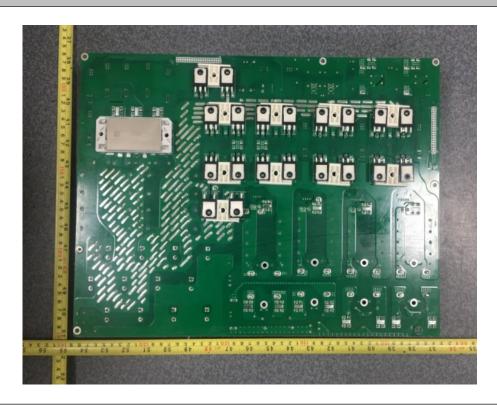


IEC 62116:2014 (50Hz)

Front side of Power board

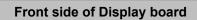


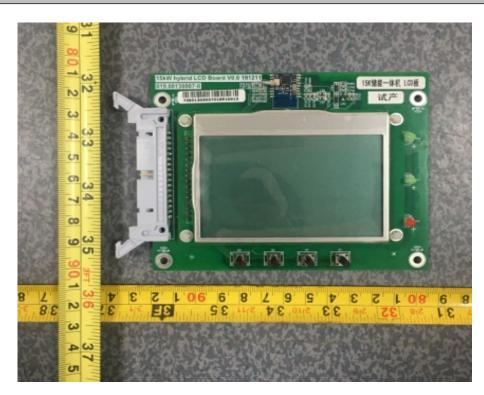
Back side of Power board



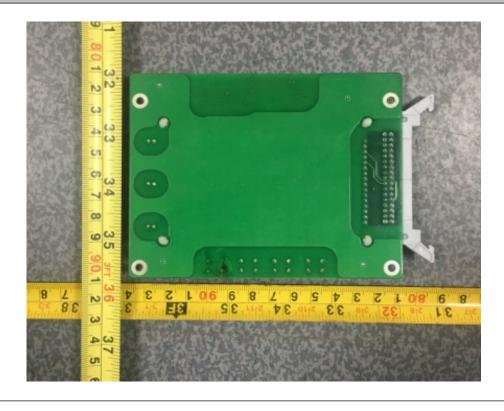


IEC 62116:2014 (50Hz)





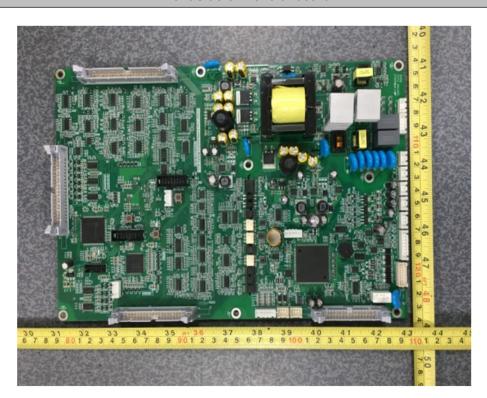
Back side of Display board



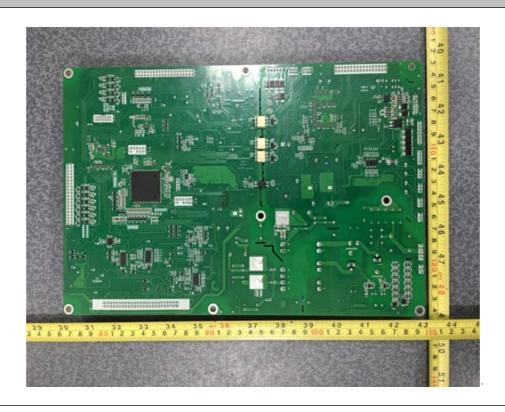


IEC 62116:2014 (50Hz)

Front side of Control board



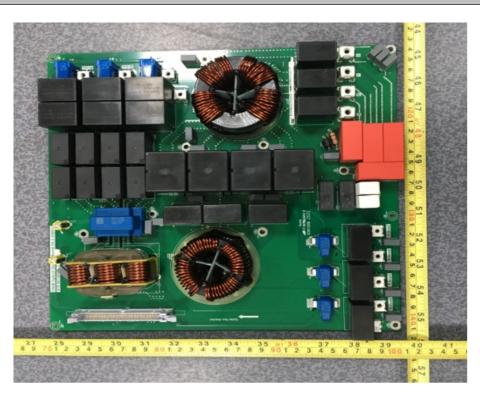
Back side of Control board



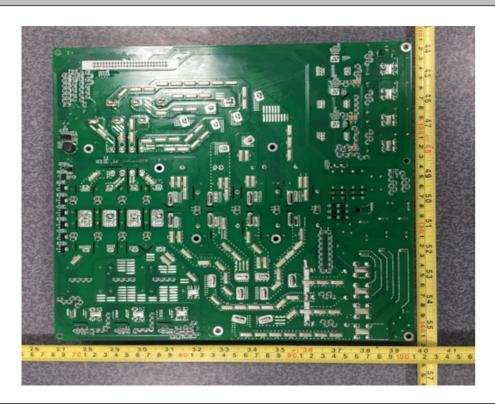


IEC 62116:2014 (50Hz)

Front side of Output board front



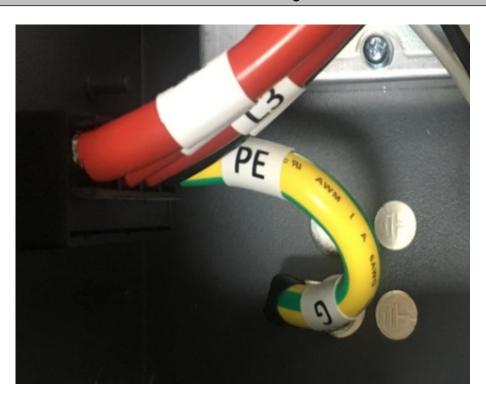
Back side of Output board front





IEC 62116:2014 (50Hz)

Grounding



Connection interface







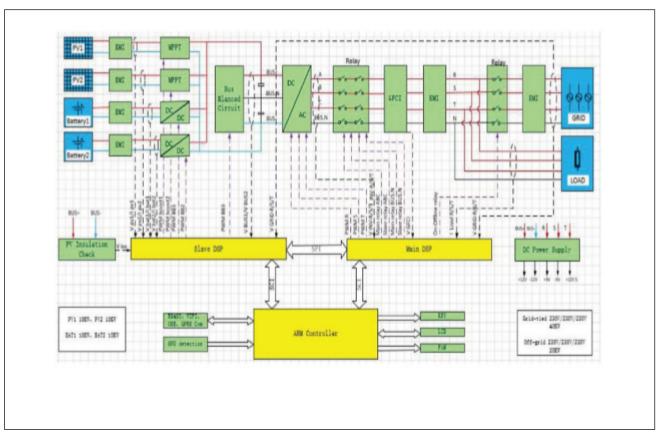
IEC 62116:2014 (50Hz)

Inverter Info(1) Product SN: SP1ES020H71002 ARM Software Version: V2.00 Main DSP Software Version: D010136 Slave DSP Software Version: D010134

Page 10 of 10

IEC 62116:2014 (50Hz)

2 ELECTRICAL SCHEMES





Page 1 of 3

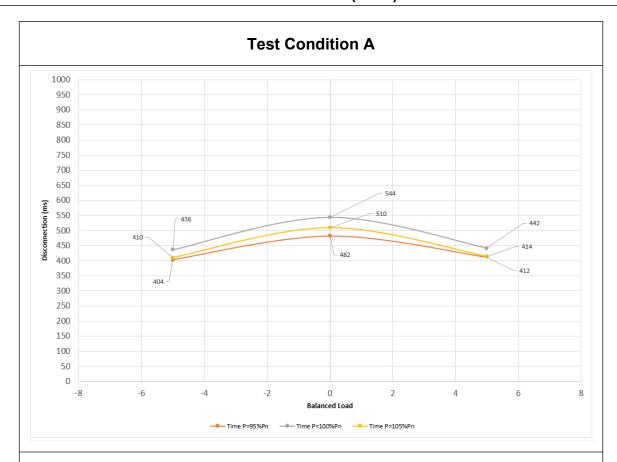
IEC 62116:2014 (50Hz)

ATTACHMENT II

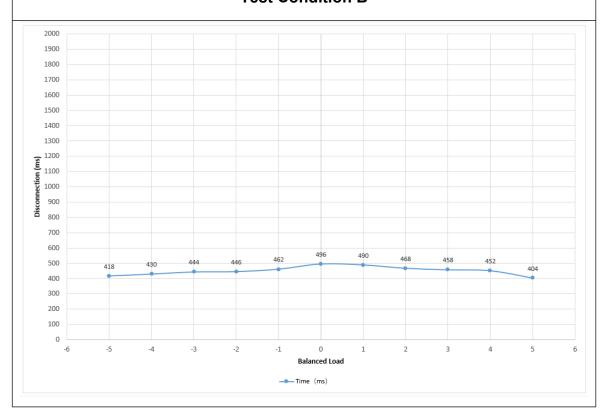
(GRAPHICS OF THE TEST RESULTS)



IEC 62116:2014 (50Hz)

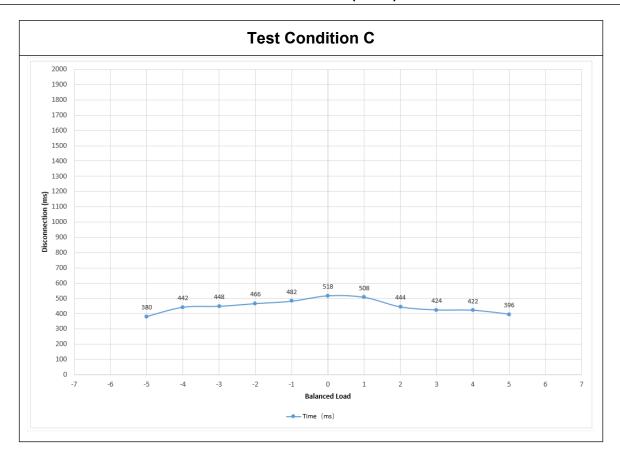


Test Condition B





Page 3 of 3





Page 1 of 19

IEC 62116:2014 (50Hz)

ATTACHMENT III

(GRAPHICS OF THE ISLANDING BEHAVIOR DETECTION)

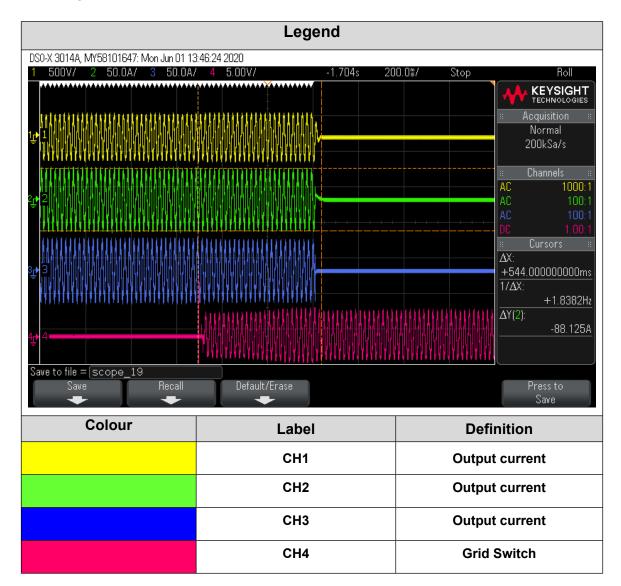
Page 2 of 19

IEC 62116:2014 (50Hz)

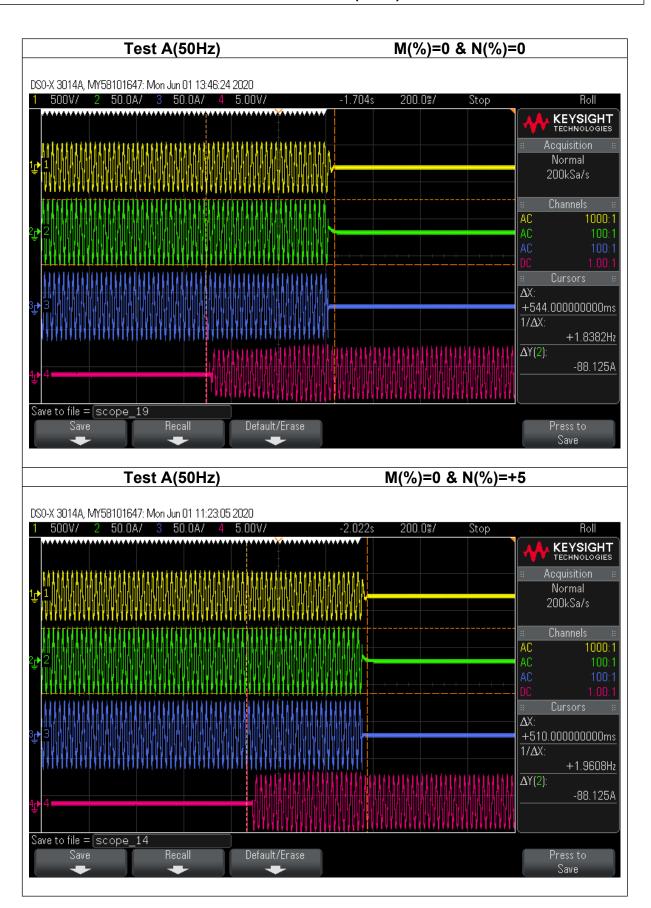
1 DEFINITIONS

- M It represents the % change in active load from nominal output power
- N It represents the % change in reactive load from nominal output power

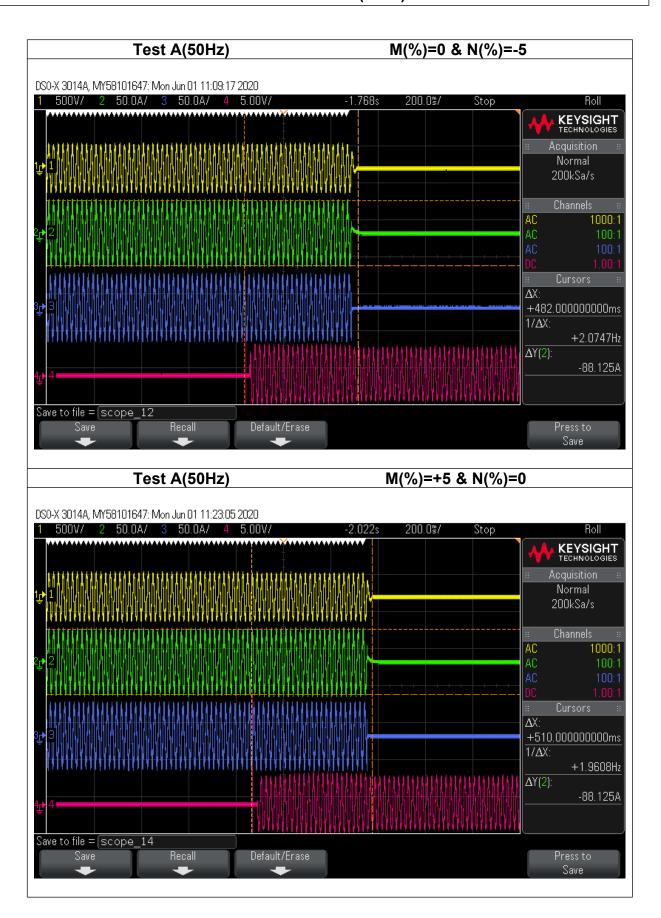
2 LEGEND



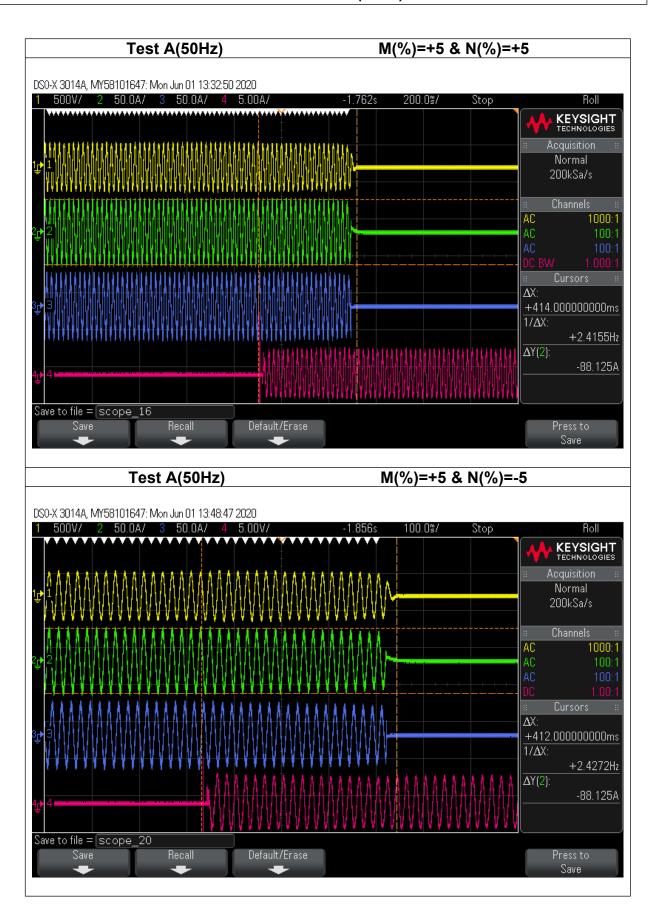




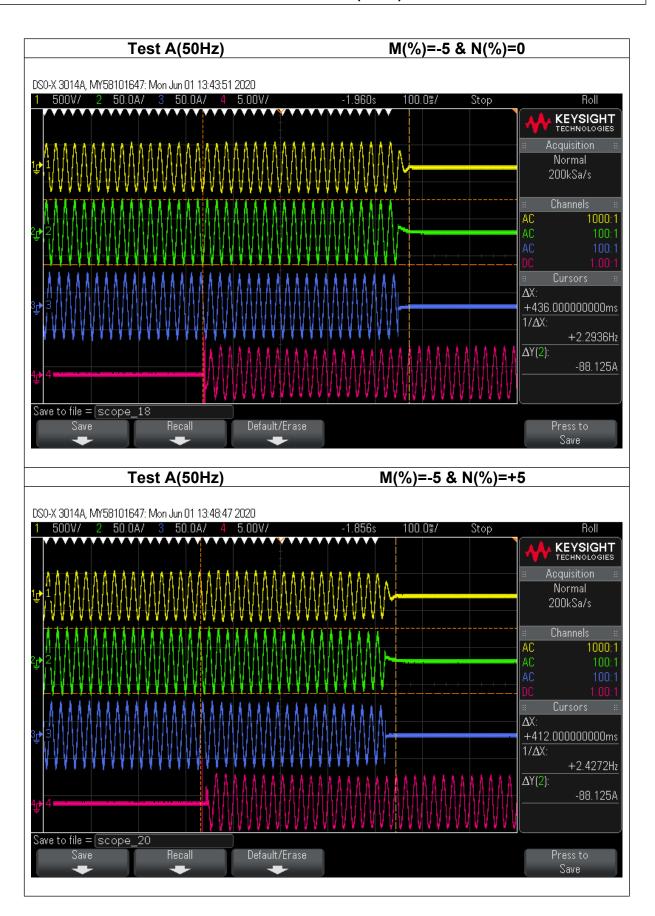




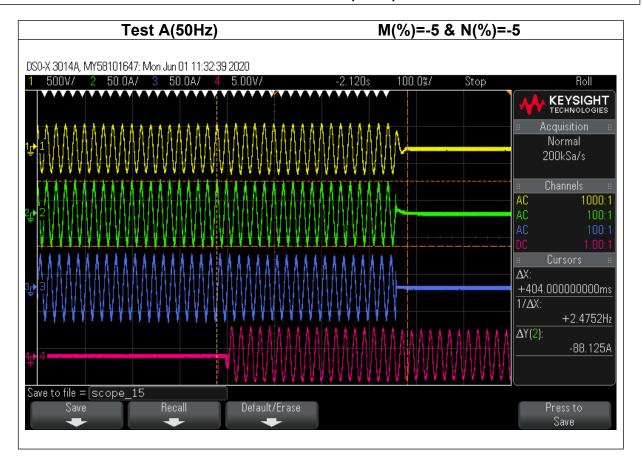




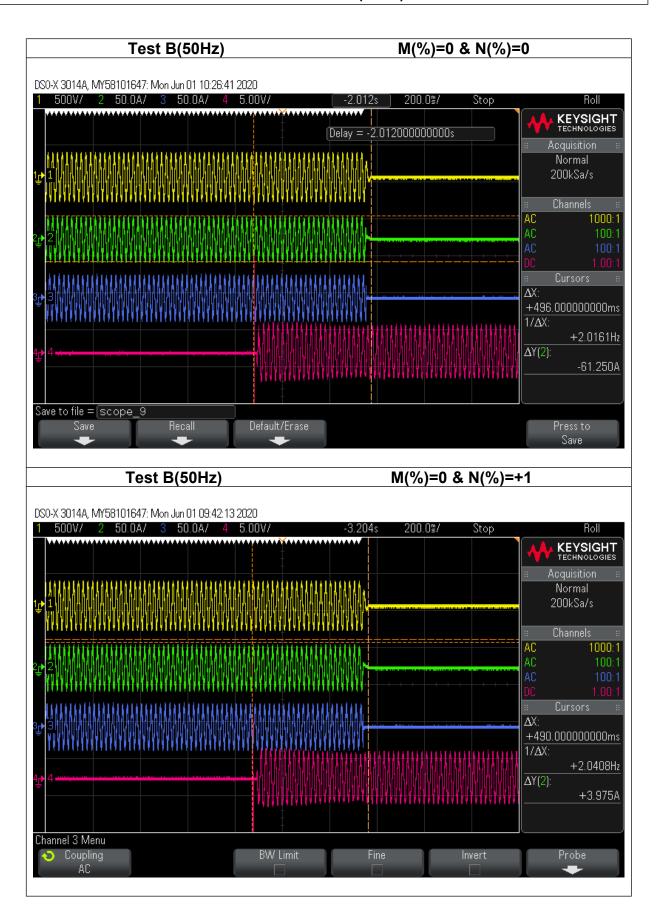




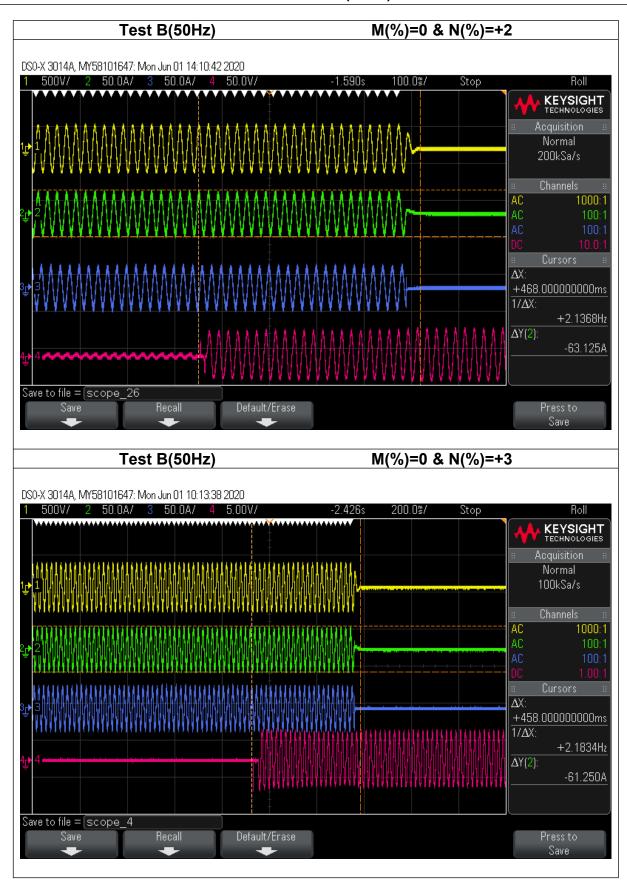
Page 7 of 19



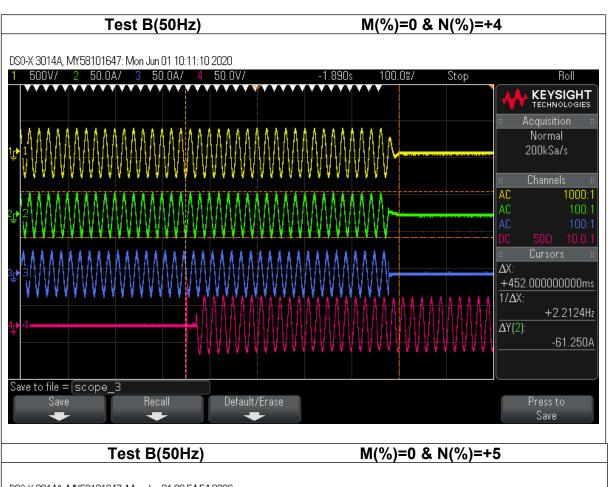


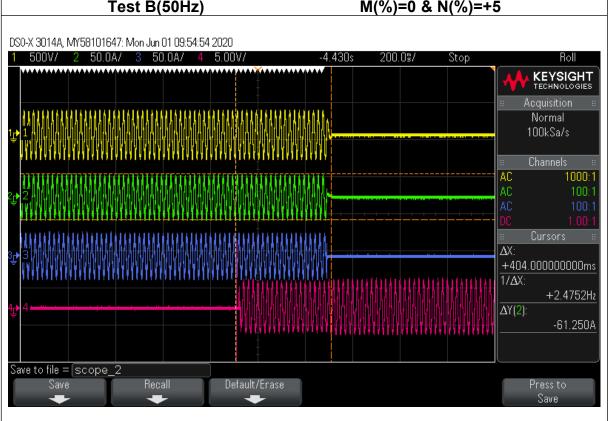




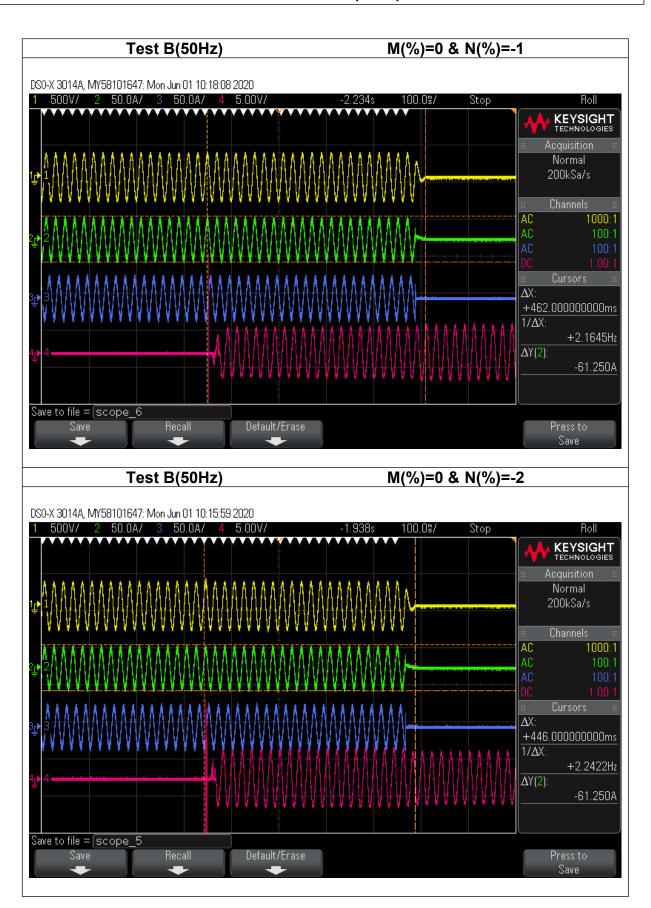




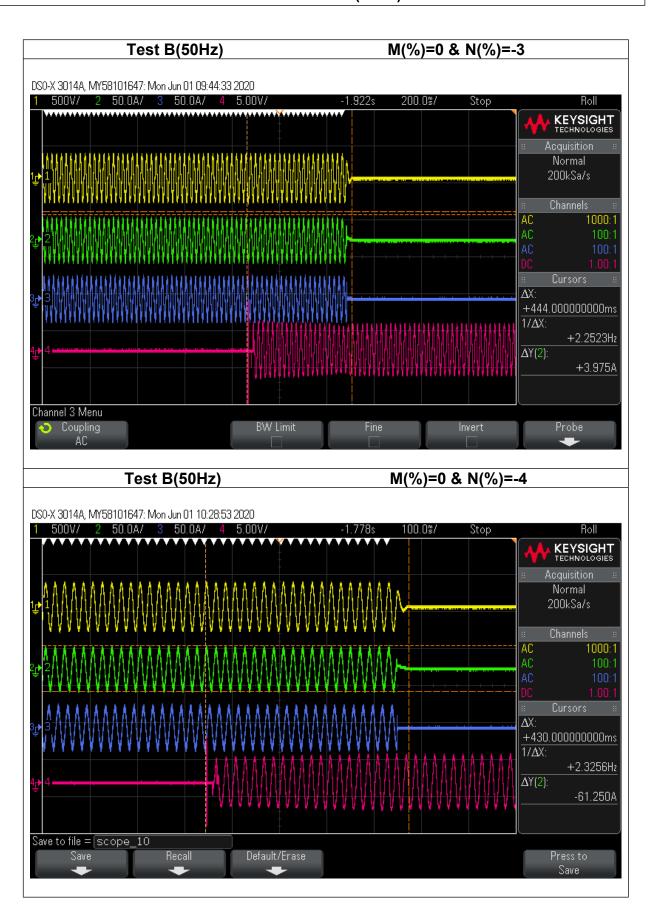


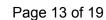






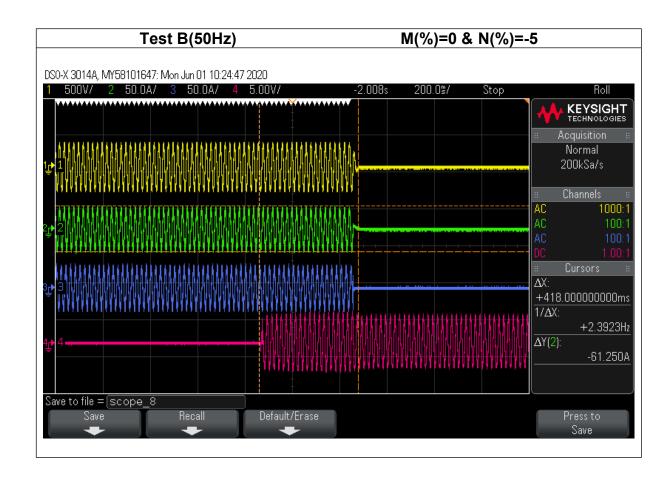




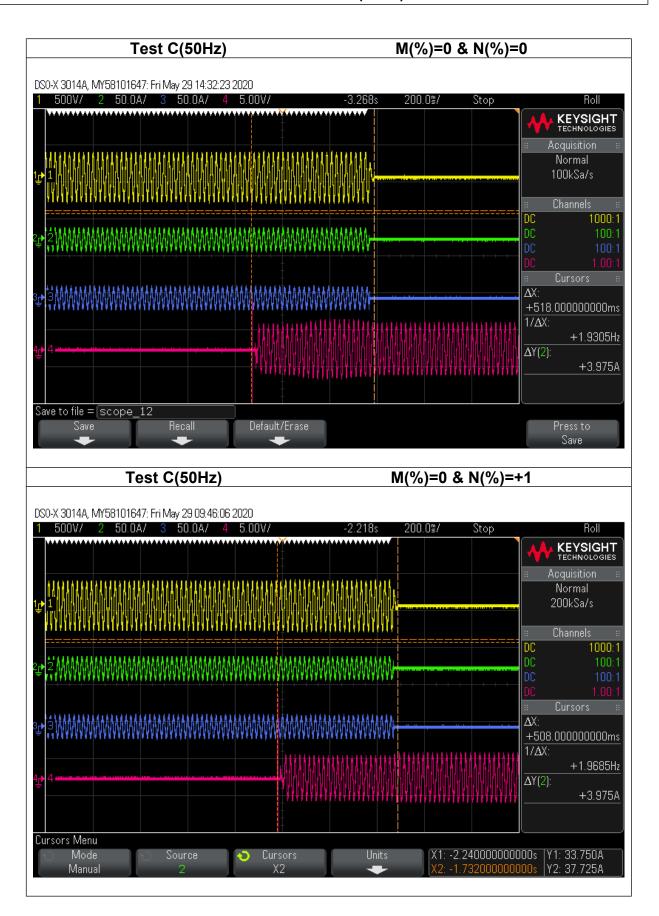


SGS

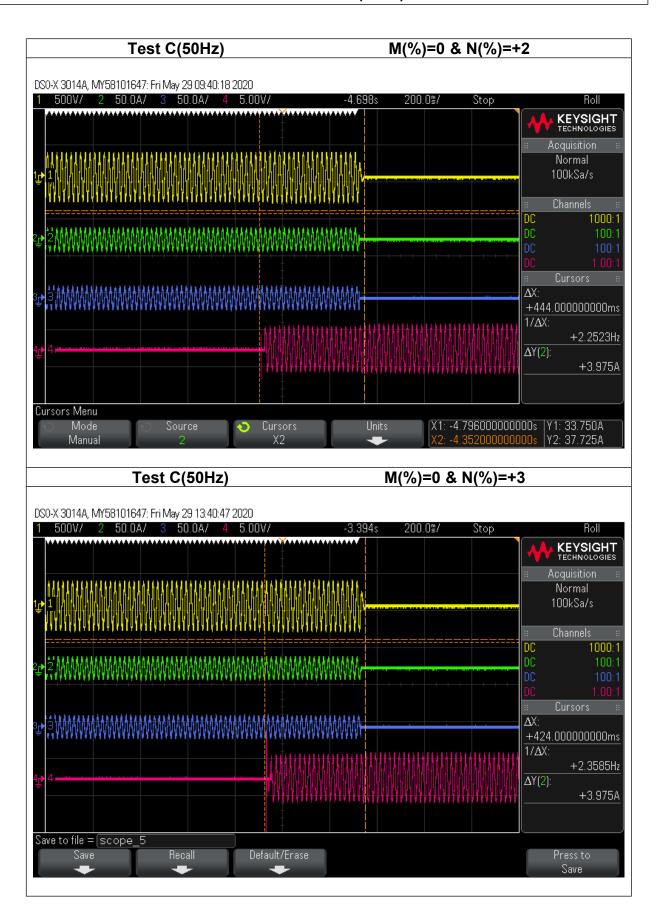
ATTACHMENT III Report N° 2219 / 0190-2



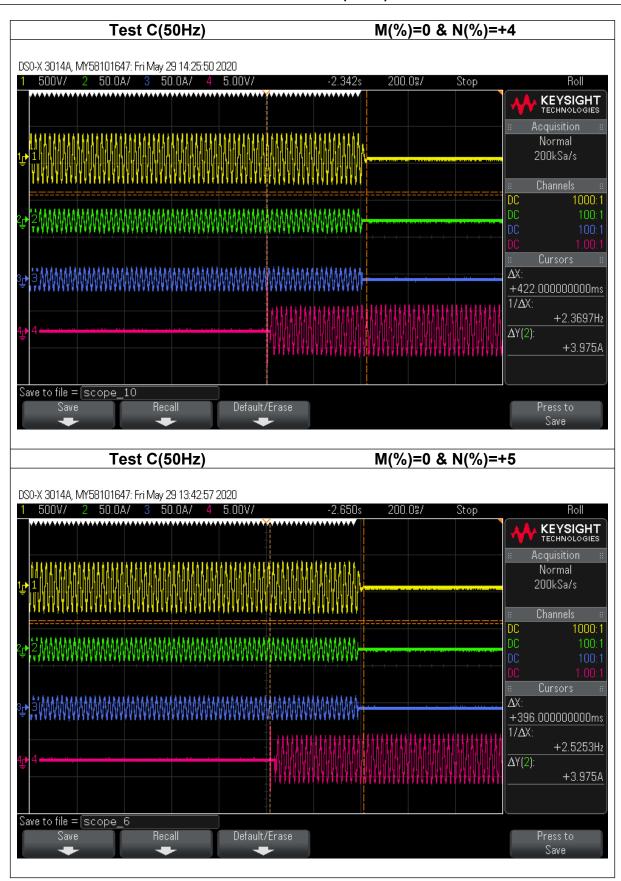




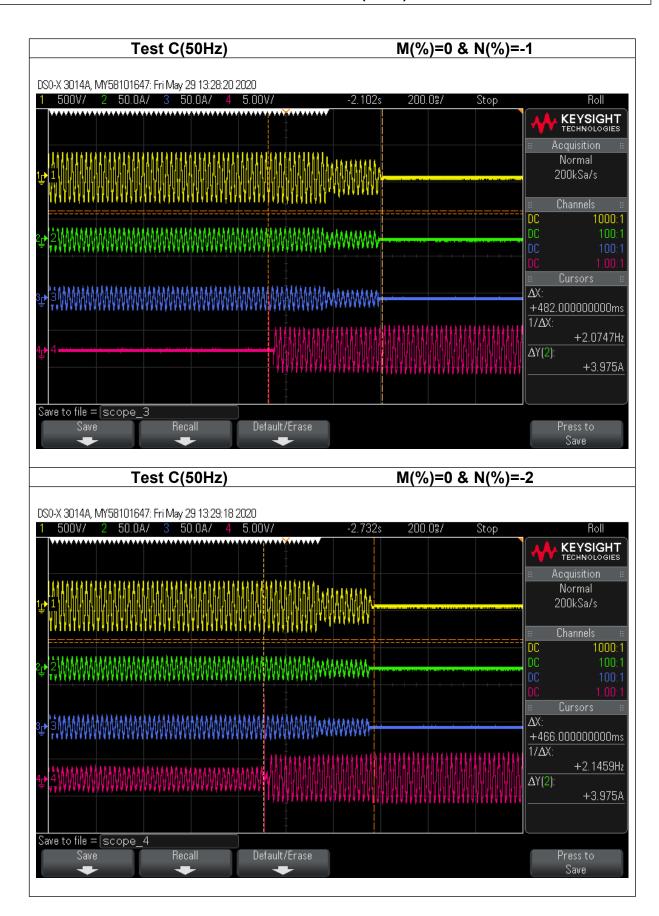




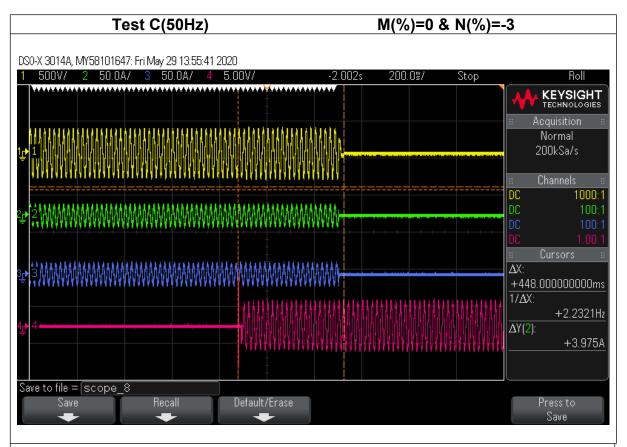


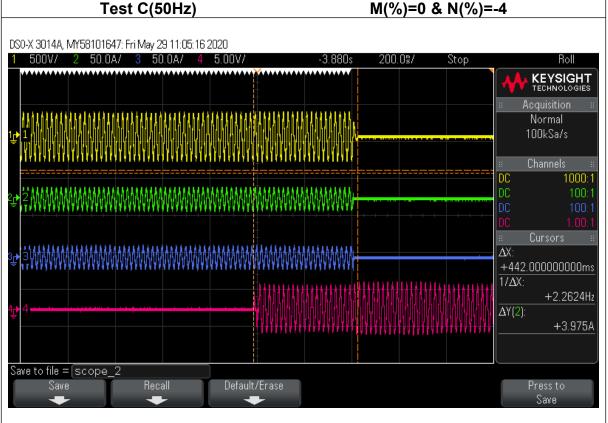




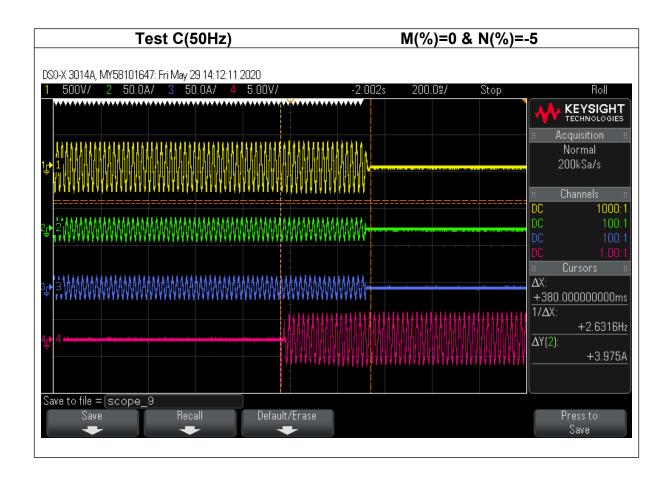








Page 19 of 19





Page 1 of 9

IEC 62116:2014 (50Hz)

ATTACHMENT IV

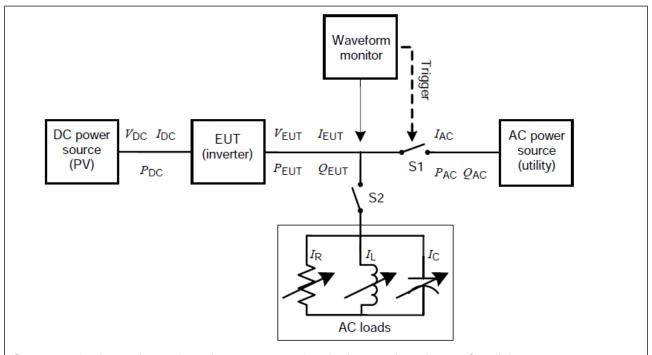
(Testing information)



Page 2 of 9

IEC 62116:2014 (50Hz)

1 TESTING CIRCUIT



Current and voltage clamps have been connected to the inverter input/output for all the tests.

All the tests and checks have been performed in accordance with the reference standard under testing.



Page 3 of 9

IEC 62116:2014 (50Hz)

2 TESTING EQUIPMENT

From	No.	Equipment Name	Model No.	Equipment No.	Calibration Date	Equipment calibration due date
	1	Digital oscilloscope	MD03024	MY58491772	2020/04/24	2021/04/23
	2	Voltage probe	SI-9110	111152	2020/1/14	2021/1/13
	3	Voltage probe	SI-9110	152627	2020/01/14	2021/01/13
Solar	4	Voltage probe	SI-9110	111134	2020/01/14	2021/01/13
far Sc	5	Power analyzer	PA5000H	C8202909082002 110001	2020/03/02	2021/03/01
Sofar	6	Current probe	CP1000A	C181000922	2020/01/14	2021/01/13
	7	Current probe	CP1000A	C181000925	2020/01/14	2021/01/13
	8	Current probe	CP1000A	C181000929	2020/01/14	2021/01/13
	9	Temperature & Humidity meter	TH101B	ZB-WSDJ-001	2020/01/14	2021/01/13
SGS	10	True RMS Multimeter	Fluke / 187	GZE012-8	2019/12/05	2020/12/04





Items	Specifications					
1) PV array simulator	,					
a) Voltage range	0 – 1000Vdc (0.01V step)					
b) Current range	0 – 40A (0.01A step)					
2) AC power source						
a) Output wiring	Three phase					
b) Output capacity	100KVA					
c) Output voltage	10-300Vrms					
d) Output frequency	45-65Hz					
e) Voltage stability	<u>+</u> 100ppm/℃					
e) Voltage stability f) Output voltage distortion 0.05% max. 3) Digital meter a) Voltage range 0 - 1000Vdc, 0 - 600Vrms b) Current range 0 - 30A c) Frequency range (accuracy) 0.2%						
3) Digital meter						
a) Voltage range	0 - 1000Vdc, 0 - 600Vrms					
b) Current range	0 – 30A					
c) Frequency range (accuracy)	0.2%					
d) Measurement items						
	· · · ·					
	Volt-ampere (VA)					
	Power factor (PF)					
	Frequency (Hz) Electric energy (Wh)					
4) Waveform recorder						
a) Sampling speed	1M/s					
b) Recording device	Memory record and USB reading					
c) Time accuracy	<u>+</u> 500ppm					
5) AC load						
a) Resistive load	Maximum voltage: 300Vrms					
	Current range: 0 – 100A					
	Capacity: 100KW					
b) Inductive load	Maximum voltage: 300Vrms					
	Current range: 0 – 100A					
	Capacity: 100KVA					
c) Capacitive load	Maximum voltage: 300Vrms					
	Current range: 0 – 100A					
	Capacity: 100KVA					



Page 3 of 9

IEC 62116:2014 (50Hz)

3 MEASUREMENT UNCERTAINTY

Voltag	e measurement uncertainty	±1.5 %
Curre	nt measurement uncertainty	±2.0 %
Frequ	ency measurement uncertainty	±0.2 %
Time	measurement uncertainty	±0.2 %
Powe	measurement uncertainty	±2.5 %
Phase	Angle	±1°
cosφ		±0.01

Note1: Measurements uncertainties showed in this table are maximum allowable uncertainties. The measurement uncertainties associated with other parameters measured during the tests are in the laboratory at disposal of the solicitant.

Note2: Where the standard requires lower uncertainties that those in this table. Most restrictive uncertainty has been considered.

4 MEASUREMENT OF AC SOURCE USED FOR TEST

Items	Desired	Measured	Deviation	Limited
Phase A Voltage(V)	230	229.8	0.2	±2%
Phase B Voltage(V)	230	229.8	0.2	±2%
Phase C Voltage(V)	230	230	0	±2%
Voltage THD (%)	<2.5%	0.03	2.47	<2.5%
Frequency	50	50	0	±0.1Hz
Phase angle distance Phase A to Phase B	120°	119.9°	0.1°	± 1.5°
Phase angle distance Phase A to Phase C	240°	240.0°	0.0°	± 1.5°



(Phase A)									
Norma1	Mode		/er:= = = : /er:= = = :	-		ate:500msec eg:Reset	EAMP	YOKOGAWA 4	•
change	items	10,	761	_	11100	eg · Nese c			
PLL	U1	Ог.	U1 [V]	hdf[%]	ΟΓ.	U1 [V]	hdf[%]	_ Σ A(3P4W)	_
Freq	49.997 Hz		229.935	400 000	dc -		0 000	U1 600Vrm	
Urms1	229.935 V	1 3	229.927 0.039	100.000 0.017	2 4	0.020 0.004	0.009 0.002	I1 30Arm	IS
Irms1	0.0000 A	5	0.033	0.006	6	0.004	0.002	U2 600Vrm	ıs
Р1	0.0000kW	7	0.007	0.003	8	0.002	0.001	12 30Arm	
S1	0.0000kva	9	0.010	0.004	10	0.008	0.004		- [
Q1	0.0000kvar	11	0.008	0.003	12	0.002	0.001	U3 600Vrm	
ኢ1 ø1	Error Error	13 15	0.005 0.001	0.002 0.000	14 16	0.002 0.003	0.001 0.002	13 30Arm	S
Uthd1	0.027 ×	17	0.006	0.003	18	0.005	0.002	Element4	
Ithd1	99.608 %	19	0.002	0.001	20	0.002	0.001	U4 600Vrm	
Pthd1	0.075 %	21	0.006	0.003		0.002	0.001	14 30Arm	S
Uthf1 Ithf1	0.026 % 148.594 %	23 25	0.003 0.005	0.001 0.002	24 26	0.017 0.015	0.008 0.006	Integ:Rese	+
Utif1	1.199	27	0.003	0.002	28	0.013	0.000	Time	`¬
	0 F	29	0.001	0.000	30	0.003	0.001	:-	-
		31	0.002	0.001	32	0.005	0.002	Timer	
		33	0.000		34	0.006	0.003	0:03:0	U
		35 37	0.002 0.003	0.001 0.001	36 38	0.003 0.002	0.001 0.001		
		39	0.003	0.000		0.003	0.001		
△ PAGE	▽ 1 ⁄7					₽AGE	▼ 1/3		
					20	_	_		
Update	35				21	020/06/12 08	3·4Z·UB		
Norma1	Mode	Uov	/er:= = = ·	-	Upda	ate:500msec	EAMP	YOKOGAWA 4	•
		Ιον	/er:= = = ·	-	Inte	eg:Reset			
change PLL	items U1	Or.	U1 [V]	hdf[%]	Ог.	U1 [V]	hdf[%]	Σ A(3P4W)	
Freq	49.997 Hz	01.	229.935	Hultza	dc -			U1 600Vrm	
		41	0.004	0.002	42	0.004	0.002	I1 30Arm	- 1
Urms1	229.935 V	43	0.002	0.001	44	0.003	0.001		-
Irms1	0.0000 A	45	0.004	0.002	46	0.005	0.002	U2 600Vrm	
P1 S1	0.0000kW 0.0000kVA	47 49	0.003 0.007	0.001 0.003	48 50	0.008 0.007	0.003 0.003	12 30Arm	15
Q1	0.0000kvar	51	0.005	0.002	52	0.005	0.002	U3 600Vrm	s
λ1	Error	53	0.002	0.001	54	0.003	0.001	13 30Arm	
Ø1	Error	55	0.003	0.001	56 50	0.004	0.002	E1	
Uthd1 Ithd1	0.027 % 99.608 %	57 59	0.001 0.004	0.001 0.002	58 60	0.004 0.002	0.002 0.001	Element4 U4 600Vrm	- I
Pthd1	0.075 %	61 -	U·UU4 		62 -			14 30Arm	
Uthf1	0.026 %								
Ithf1	148.594 %			I				_Integ:Rese	$\mathbf{t}_{_}$
Utif1	1.199	٠.						Time	_
16111	0 F	69 - 71 -						Timer	
								0:03:0	0
		75 -			76 -				_
					78 -				
		79 -			80 -				
△ PAGE	▽ 1 ∠7					⊸ naer	▼ 2/3		
					_	_	_		
Update	35				20	020/06/12 08	3:42:22		



(Phase B)									
Norw-	l Mada	11	.or' = = =	_	T 4_ *	3 : 30Arms		VOKOCAINA 🍝	
Normal	i Mode		rer:= = =	-		3∶ JUARMS eg∶Reset		YOKOGAWA ◆	
	e items								
PLL	U1 50.002 Hz	Or .	U2 [V] 229.833	hdf[%]	qc -	U2 [V]	hdf[%]	ΣΑ(3P4W) [U1 600Vrms]	
Freq	30.002 HZ	1	229.827	100.000	2	0.010	0.004	I1 30Arms	
Urms2	229.833 V	3	0.048	0.021	4	0.005	0.002		
Irms2	0.0000 A	5	0.016	0.007	6	0.006	0.003	U2 600Vrms	
P2	-0.0000kW	7	0.008	0.003	8	0.005	0.002	I2 30Arms	
S2	0.0000kVA	9	0.007	0.003		0.004	0.002	113 60014	
Q2 λ2	0.0000kva Error	r 11 13	0.003 0.007	0.001 0.003		0.004 0.004	0.002 0.002	U3 600Vrms I3 30Arms	
ø 2	Error	15	0.001	0.000		0.002	0.001	15 SONTING	
Uthd2	0.027 ×	17	0.007	0.003	18	0.001	0.000	_ Element4	
I thd2	99.655 %	19	0.002	0.001		0.006	0.003	U4 600Vrms	
Pthd2 Uthf2	0.029 % 0.023 %	21	0.001 0.002	0.000 0.001		0.000 0.005	0.000	I4 30Arms	
Ithf2	149.869 %	23	0.002	0.001		0.003	0.002 0.002	Integ:Reset	
Utif2	1.117	27	0.002	0.001		0.004	0.002	Time	
	0 F	29	0.002	0.001	30	0.002	0.001	:	
		31	0.003	0.001		0.002	0.001	Timer	
		33 35	0.008 0.004	0.004		0.002 0.003	0.001 0.001	0:03:00	
		37	0.004	0.002 0.000		0.003	0.001		
		39	0.003	0.001		0.003	0.001		
	E▽ 2/7					_	E▼ 1/3		
Update	6				20	120/06/12 1	4:47:32		
Normal	Mode		er:= = =	-		3 : 30Arm	s	YOKOGAWA ◆	
change	ítems	1000	er:= = =	_	Int	eg:Reset			
PLL	U1 [Ог.	U2 [V]	hdf[%]	Or.	U2 [V]	hdf[%]	Σ A(3P4W)	
Freq	50.002 Hz		229.833		dc			[U1 600Vrms]	
		41	0.006	0.002		0.003	0.001	I1 30Arms	
Urms2	229.833 V	43	0.003	0.001		0.003	0.001		
Irms2 P2	0.0000 A -0.0000kW	45 47	0.007 0.004	0.003 0.002	46 48	0.005 0.001	0.002 0.000	U2 600Vrms 12 30Arms	
S2	0.0000kW	49	0.004	0.002		0.004	0.002	12 JUATINS	
Q2	0.0000kvar	51	0.006	0.003		0.002	0.001	U3 600Vrms	
λ2	Error	53	0.006	0.003	54	0.004	0.002	I3 30Arms	
Φ2	Error	55	0.004	0.002		0.003	0.001		
Uthd2	0.027 %	57	0.002	0.001	58	0.007	0.003		
Ithd2	99.655 %	59 61	0.007	0.003		0.003 	0.001	U4 600Vrms I4 30Arms	
Pthd2 Uthf2	0.029 % 0.023 %							I4 30Arms	
Ithf2	149.869 %	65			66			Integ:Reset	
Utif2	1.117	67			68			Time	
Itif2 -	o F								
								Timer	
								0:03:00	
		79			80				
								•	
△PAGE▽						_	GE ▼ 2∕3		
Update	6				2	020/06/12	14:47:37		



				(Phase	.0,			
Norma	1 Mode	Uov	/er:= = =	-	I 1-:	3 : 30Arms		YOKOGAWA ◆
			/er:= = =	-		eg:Reset		
change PLL	e items U1		U3 [V]	hdf[%]	Ог.	U3 [V]	hdf[%]	Σ A(3P4W)
Freq	50.002 Hz	Or.	229.951	IIU I L7.3	dc ·	03 141		U1 600Vrms
	50.002 HE	1	229.950	100.000	2	0.034	0.015	I1 30Arms
Urms3	229.951 V	3	0.037	0.016	4	0.006	0.003	1
Irms3	0.0000 A	5	0.016	0.007	6	0.001	0.000	U2 600Vrms
P3 S3	0.0000kW 0.0000kva	7 9	0.010 0.003	0.004 0.001	8 10	0.001 0.001	0.001 0.000	I2 30Arms
Q3	0.0000kva 0.0000kva		0.003	0.001		0.001	0.000	U3 600Vrms
λ3	Error	13	0.003	0.001		0.003	0.001	I3 30Arms
ф3	Error	15	0.001	0.000		0.001	0.001	
Uthd3	0.027 %	17	0.005	0.002		0.004	0.002	Element4
Ithd3 Pthd3	98.724 % 0.010 %	19 21	0.007 0.007	0.003 0.003		0.003 0.004	0.001 0.002	U4 600Vrms I4 30Arms
Uthf3	0.024 %	23	0.007	0.001		0.003	0.002	14 JUATINS
Ithf3	155.307 ×	25	0.003	0.001		0.004	0.002	Integ:Reset
Utif3	1 . 155	27	0.010	0.005		0.003	0.001	Time
Itif3	0 F	29	0.004	0.002		0.003	0.001	:
		31 33	0.003 0.008	0.001 0.003		0.003 0.003	0.001 0.001	Timer 0:03:00
		35	0.003	0.001		0.003	0.001	0.03.00
		37	0.002	0.001		0.002	0.001	
		39	0.002	0.001	40	0.001	0.001	
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						_		
Update	6				20	120/06/12 1	4:47:51	
Norma1	Mode		er:= = = : er:= = = :	-		3 : 30Arm eg:Reset	s	YOKOGAWA ◆
change								
PLL	U1	0г.	U3 [V]	hdf[%]	Or .	N3 [A]	hdf[%]	Σ A(3P4W)
Freq	50.002 Hz	41	229.951 0.004	0.002	dc 42	0.003	0.001	U1 600Vrms I1 30Arms
Urms3	229.951 V	43	0.004			0.003	0.003	III JUATINS
Irms3	0.0000 A	45	0.010	0.004		0.003	0.001	U2 600Vrms
Р3	0.0000kw	47	0.007	0.003	48	0.006	0.002	I2 30Arms
S3	0.0000kva	49	0.005			0.003	0.001	
Q3	0.0000kvar	51 53	0.003	0.001		0.005	0.002	U3 600Vrms
አ3 ø3	Error Error	55	0.002 0.003	0.001 0.001		0.006 0.001	0.003 0.000	I3 30Arms
Uthd3	0.027 %	57	0.005	0.002	58	0.001	0.003	Element4
Ithd3	98.724 %	59	0.004	0.002	60	0.003	0.001	U4 600Vrms
Pthd3	0.010 ×	61 -			62			I4 30Arms
Uthf3	0.024 %	63 -						
Ithf3	155.307 %	67			66			Integ:Reset
Utif3 Itif3 -	1.155 o F			I				Time
16113	٠. ا			I				Timer
		73 -						0:03:00
		75 -						
		77 -						
	l	79 -			80			
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Update	6				2	020/06/12	14:47:55	

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ATTACHMENT IV Report N° GZES200601936102

